RLC Example

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Example: ex_RLC

Description:

This is a simple design containing a resistor, inductor and capacitor driven by an ideal voltage source. The models are written completely in the VHDL-AMS modeling language (use the **RMB > Push Language > VHDL** to view the source files). The purpose of this example is to show how electrical building blocks can be easily written in VHDL-AMS and simulated in SystemVision. A picture of the schematic is shown below:

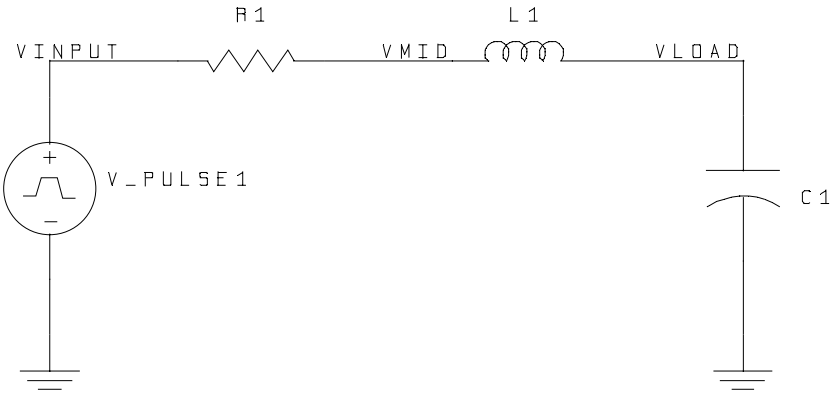

Figure 1- RLC circuit

Getting Started

Users are encouraged to look through the following documents from the SystemVision Help menu. (The RLC example is also used in the ***Getting Started with SystemVision*** tutorial.)

- **Help > SystemVision Help Topics**
  This is the main online help resource with hyperlinks. Topics include: Introduction to SystemVision, The User Interface, SystemVision Commands, and "How do I …?" tips.
- **Help > SystemVision Online Manuals > Getting Started**
  The Getting Started tutorial is provided to acquaint users with SystemVision. It is recommended that users run through this tutorial prior to running other examples.
- **Help > SystemVision Online Manuals > User's Manual**
  The Users Manual is provided as a reference source for SystemVision. Detailed explanations on tool usage are provided.
- **Help > SystemVision OnlineManuals > SystemVision Quick Reference Guide**
  This document should be printed and used as a reference for running SystemVision examples.
- **Help > SystemVision Online Manuals > VHDL-AMS Quick Reference Guide**
  This VHDL-AMS reference succinctly reviews many VHDL-AMS language features. It is intended for those users interested in creating/understanding VHDL-AMS models.

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- For specific information on the Waveform Viewer, select **Help > Quick Start and Help > Tutorial > Open Tutorial** from the main Waveform Viewer window).

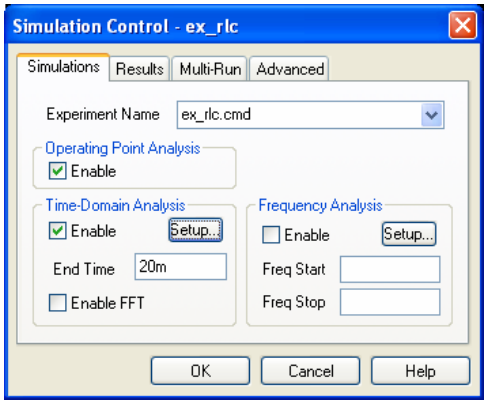
A brief summary of the basic steps required to simulate the RLC circuit is given below, as well as some design exploration suggestions.

Design Selection/Viewing/Editing

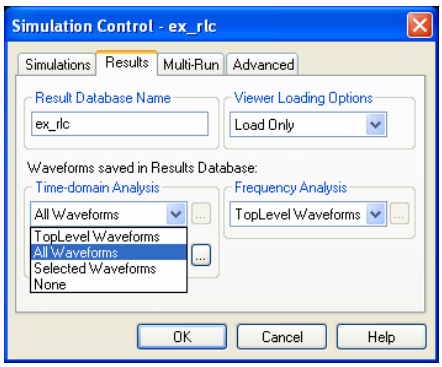
1. Make sure the **ex_RLC** project is loaded into SystemVision.
2. From the **Project** tab, click on **Design Roots > ex_rlc** to open the schematic.

Simulating the circuit

1. From the Pull-down menu, select **Simulation > Simulate** to invoke the Simulation Control window (there is also a simulation icon available on the iconbar). The VHDL-AMS files will be compiled as necessary.
   - ✓ The **Simulations** tab is for the basic settings and to enable/disable the desired analyses. Enable the **Time-Domain Analysis** and set **End Time** to **20m** as shown:



   - ✓ The **Results** tab is used to select the signals for viewing. The default selection is **TopLevel Waveforms** which will save all signals at the highest level of hierarchy. Since this is a small design, **All Signals** was selected for convenience. You can also choose **Selected Waveforms** and click on the browse button (**...**) to select individual signals.



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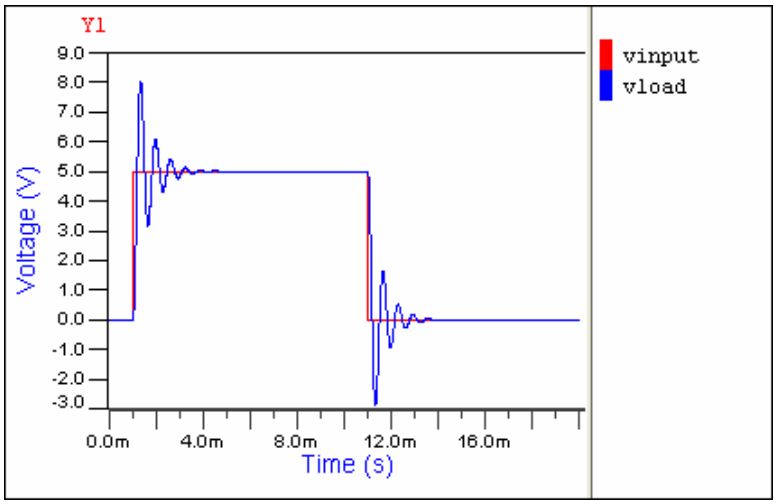
- ✓ The **Multi-Run** tab is for performing parametric variations (more on this later)
- ✓ The **Advanced** tab is used for advanced simulation settings (normally not required).

2. Click the **OK** button to run the simulation (the **Output Window** will display the simulation progress and any error messages that may be issued).

Viewing Results

1. The simulation results will automatically be loaded into the waveform viewer upon completion of a successful simulation (if not, look in the **Output Window** for any error messages).
2. Individual signals can be viewed by double-clicking with the LMB or by using the drag-and-drop feature. You can also plot a signal from the schematic by selecting the desired signal and using **RMB > Plot Waveform**. Use one of these methods to plot the signals **vinput** and **vload** which should appear as shown below:



3. Look at any other signals of interest. Additional waveform viewing features are summarized below:
   - ✓ Multiple graph windows and workspaces can be easily created using the menus or drag-and-drop.
   - ✓ Signals can be deleted using the **Delete** key on your keyboard, or by using the **RMB > Delete** command on the signal name.
   - ✓ Markers can be place to view waveform coordinates
   - ✓ The **Measurement Tool** can be used to measure various waveform characteristics (more on this later)

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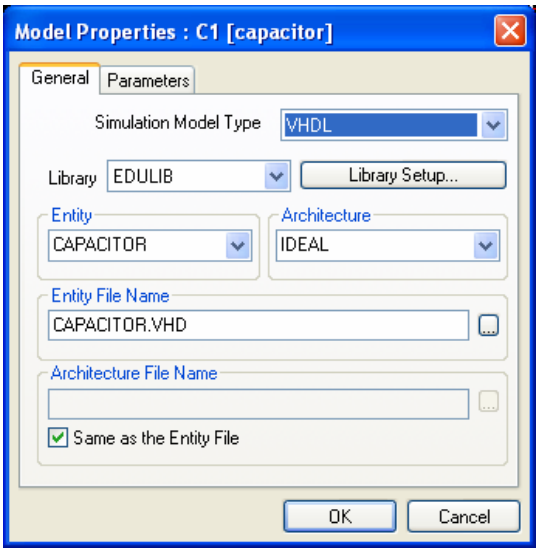
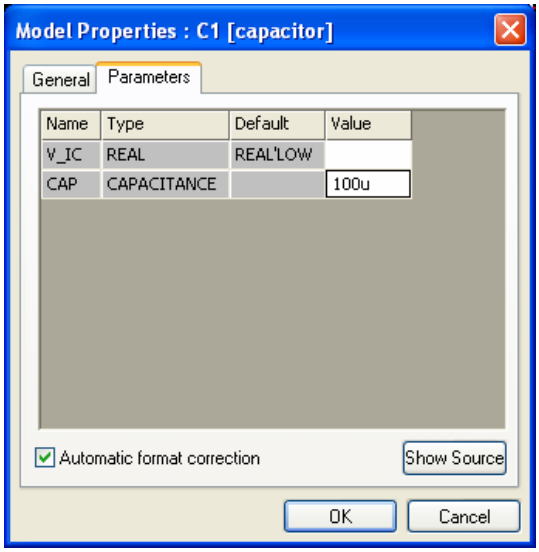
Modifying the Design

With SystemVision it is easy to modify design parameters, re-simulate and compare results. To illustrate this, let's alter the capacitor value.

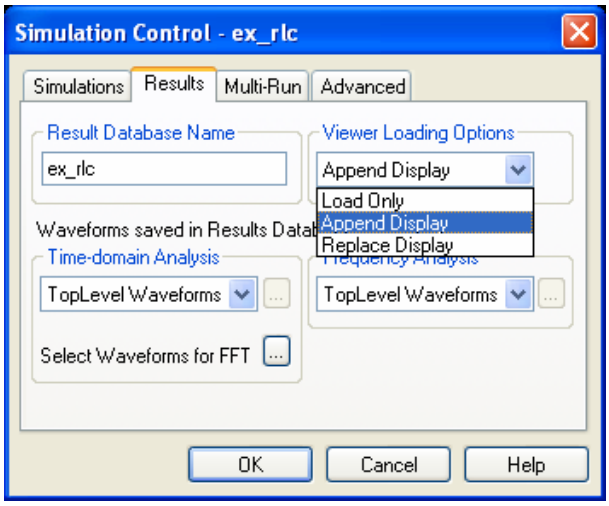
1. Select the capacitor and select **RMB > Edit Model Properties**. This will bring up the **Model Properties** dialog:





The **General** tab displays information on the VHDL-AMS library, entity, architecture, and file name. The **Parameters** tab allows you to change the value of any VHDL generic (parameter).

2. Change the **CAP** value to **100u** as shown above and re-simulate.
3. When the simulation dialog appears, select the **Results** tab and change the **Viewer Loading Options** to **Append Display** as shown below:



4. The new results will be automatically appended to your active graph.

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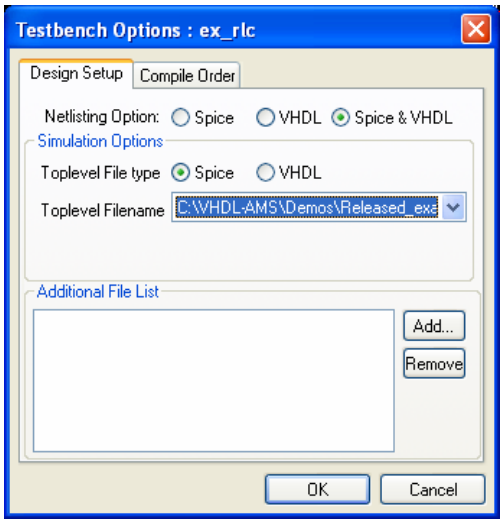
Sweeping Parameters

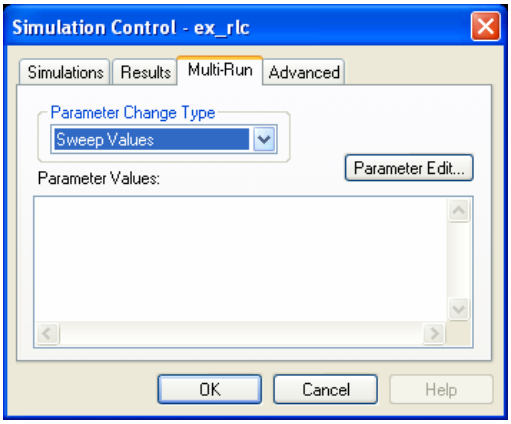
With SystemVision it is also possible to automatically sweep parameters over a specified range. Doing so however requires you to switch to the "Spice-on-top" mode (see Simulating with Spice tutorial for more details). Before simulating, SystemVision generates a netlist which is sent to the simulator for processing. This netlist can be either in VHDL-AMS or SPICE format. For a nominal simulation, there is no difference as to which netlist is used, but in order to sweep parameters, you must use a Spice netlist. To change the netlist format, select **Simulation > Testbench Options** from the pulldown menu to display the following dialog:



From this dialog set the **Toplevel File Type** to **Spice** (you may still generate both Spice and VHDL netlists is desired)

Setting up Parametric Sweeps

1. Click **Simulation > Simulate** to invoke the **Simulation Control** dialog
2. Click on the **Multli-Run** tab and change **Parameter Change Type** to **Sweep Values** as shown below:



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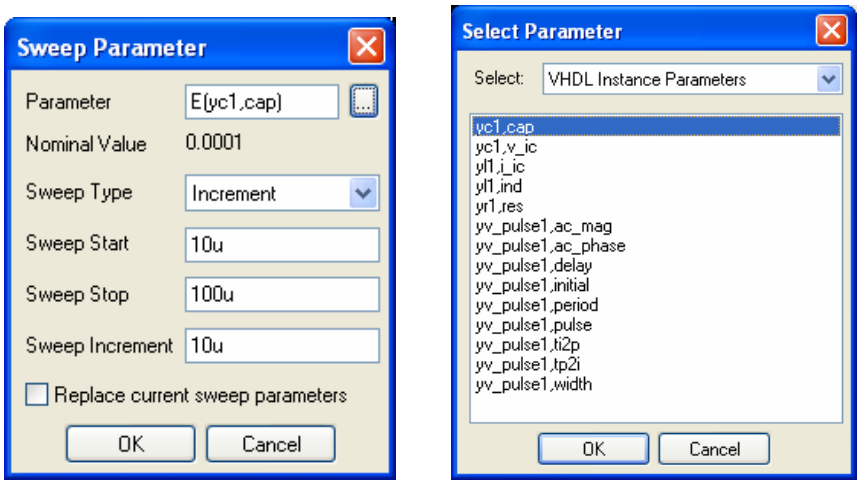
3. Click on the **Parameter Edit** button to invoke the **Sweep Parameter** dialog:

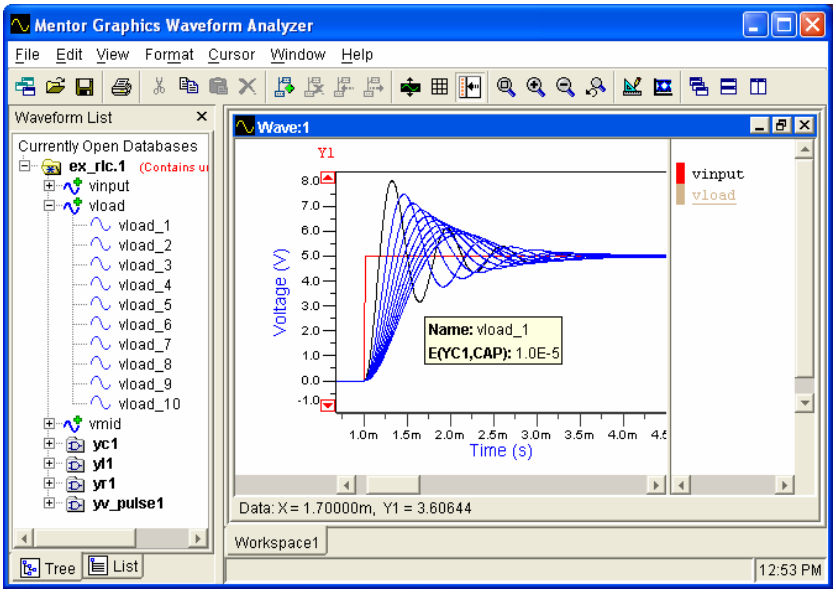


4. Click on the browse button (**...**) to select the capacitance (**yc1,cap**). Note: Since this design consists exclusively of VHDL-AMS models, you need to set the **Select** field to **VHDL Instance Parameters**.
5. Fill in the rest of the **Sweep Parameter** dialog as shown above and select **OK** to continue.
6. The **Simulation Control** dialog will be automatically updated with the sweep information. Click **OK** to continue with the simulation. The output window will display the progress of each simulation run.

Viewing Multi-Run Results

Again, the results will automatically be loaded into the waveform viewer. They will be in the form of compound (multi-member) waveforms.

1. Plot the signal **vload** as shown below (use **LMB** to zoom in):



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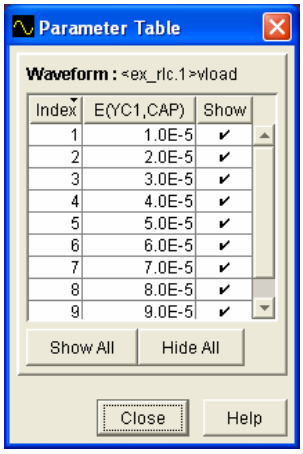
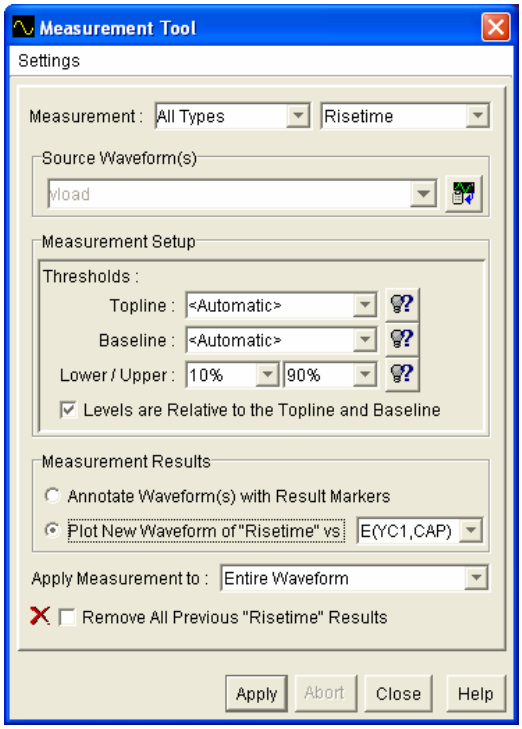
2. The **+** sign and symbol next to the signal name indicates it is a compound waveform. Each member can also be displayed by clicking on the **+** sign to expand and plotting individually.
3. Placing your cursor over one of the members in the graph area will display the individual member name along with the parameter value(s) used for that simulation run as shown above.
4. Placing your cursor over the signal name and selecting **RMB > Parameter Table ...** will allow you to view the parameter values for all the runs:



Performing a Measurement

1. Click on the **Measurement Tool** in the toolbar to bring up the measurement dialog:



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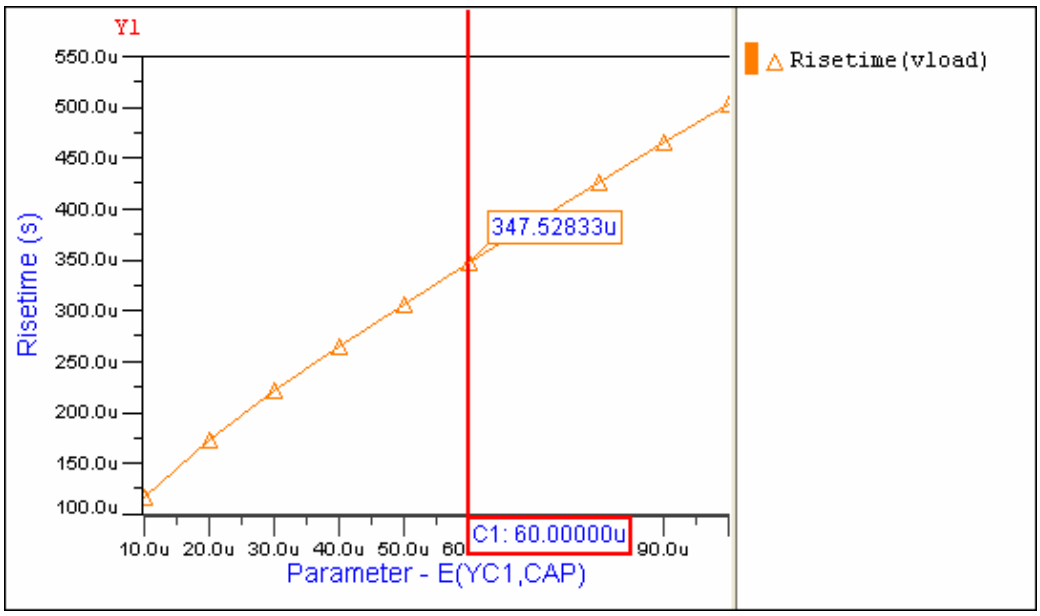
2. Select the **Risetime** measurement from the pulldown list.
3. Set the **Source Wavewform** to the compound waveform **vload.**
4. Leave the thresholds set at automatic.
5. Select **Annotate Waveforms ...** to annotate the graph with a measurement marker and click **Apply**.
6. Note the marker can be moved from one member to the next.
7. Move your cursor over the marker and select **RMB > Measurement Results** to view a table of the measurement results.
8. Return to the **Measurement Tool** and select **Plot New Waveform ...**
9. Click **Apply** will display a new waveform as shown below:



10. This automatically calculates the risetime of each individual member and plots it as a function of the capacitance. Placing a cursor will display the risetime and associated capacitance value.

Performing a Frequency Analysis

With SystemVision it is also possible to perform a small-signal frequency (AC) analysis. Before running a frequency analysis, you will need to add an AC component to the voltage source. Typically, this involves normalizing the AC magnitude to 1 and AC phase to 0 for the desired input.

1. Select the voltage source on the schematic.
2. Select **RMB > Edit Model Properties** to invoke the model properties dialog.

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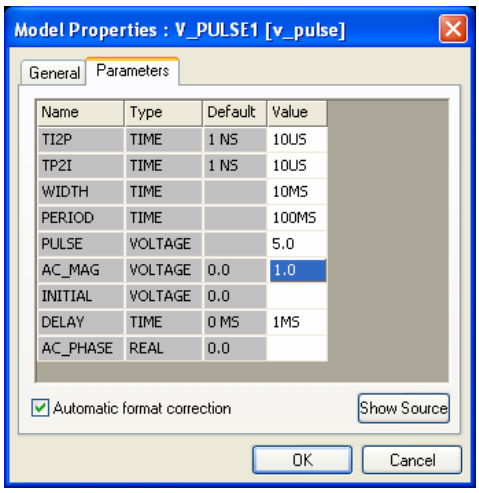
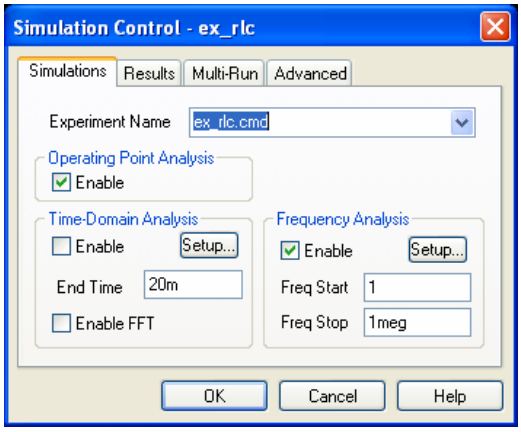
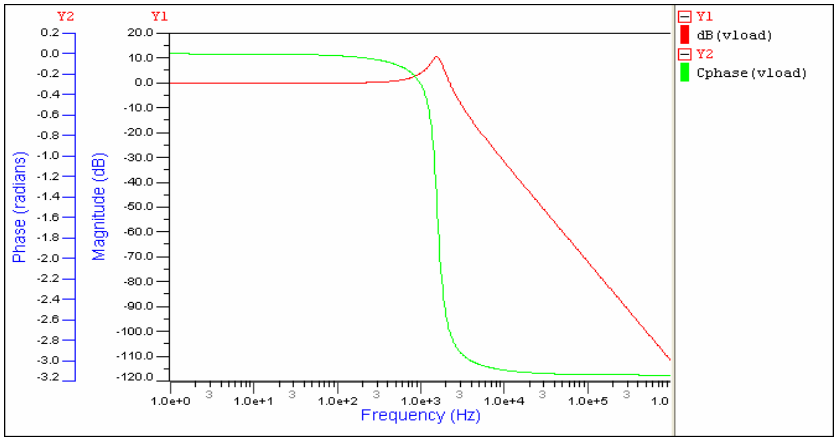


3. Click on the **Parameters** tab, set **AC_MAG** to **1**, and select **OK**.
4. Re-invoke the **Simulation Control** dialog.



5. Enable the **Frequency Analysis** and run from **1** to **1meg** (frequency units are Hz).
6. Be sure to disable the parameter sweep in the **Multi-Run** tab.
7. Click **OK** to run the analysis.
8. Plot the signal **vload** to see the frequency response:



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